

Automated Wafer-Level Edge Coupling Test Guidelines for Photonic Integrated Circuits (Rev 3.4)

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Abstract

As photonic integrated circuits (PICs) emerge at the forefront of high-speed data communication and optical computing [Refs. 1,2], the need for robust, repeatable, and high-throughput wafer-level testing grows in urgency. However, the unique nature of optical interfaces, mechanical alignment sensitivity, and test system interactions present a new set of challenges unfamiliar to traditional electrical wafer-level testing workflows. This paper outlines the common pain points encountered during the transition into wafer-level PIC testing, serving as a primer for test engineers in semiconductor environments.

At Sunyu Photonics, we have developed a dedicated wafer-level tester powered by proprietary calibration processes and algorithms. The system achieves state-of-the-art repeatability, with run-to-run variation under 0.1 dB and load-to-load variation under 0.2 dB, based on the standard deviation of insertion loss. It completed 520 test points in 125 minutes—averaging 14 seconds per point, including stage movement, fiber alignment, and wavelength sweeps. These results show that the Sunyu system is well-suited for both advanced R&D and high-throughput production, providing a robust and scalable solution for wafer-level photonic testing.

1. Introduction

Photonic Integrated Circuits (PICs) have revolutionized on-chip optical data transmission by integrating lasers, modulators, and detectors into compact, scalable platforms. Unlike their electronic counterparts, PICs require precise optical alignment for signal coupling, introducing a new class of mechanical, optical, and environmental constraints at the wafer level. Test engineers accustomed to electrical probing face a steep learning curve.

2. Optical Probe

Unlike traditional metal probe contacts used in electrical testing, photonic I/O ports require sub-micron precision and angular accuracy in three dimensions to achieve reliable optical coupling. At the wafer level, this introduces a level of mechanical and optical complexity that significantly exceeds that of standard electrical probing.

Several wafer-level optical probing strategies - such as the use of planar lightwave circuit (PLC) [Ref. 3], polished Fiber Array Units (FAUs) [Refs. 4,5], 3-D printed lensed fibers [Refs. 6,7] have been proposed for coupling light into photonic integrated circuits (PICs).

Among the available optical probe options, the polished FAU offers significant advantages in cost-effectiveness and reliability, making it well-suited for wafer-level automated testing. Figure 1 illustrates a typical configuration where a polished FAU is used as the optical probe for PIC wafer testing. A key benefit of the polished FAU

is its shallow insertion depth, typically only 10–20 μm into the coupling trench, depending on the Z-position of the edge couplers. This allows for trench dimensions as small as 100 μm in width and 50 μm in depth, significantly simplifying the trench-etching process and reducing fabrication cost. The FAU can be safely aligned and held at a working distance of 10–15 μm from the trench wall, minimizing the risk of contact or damage during automated operation.

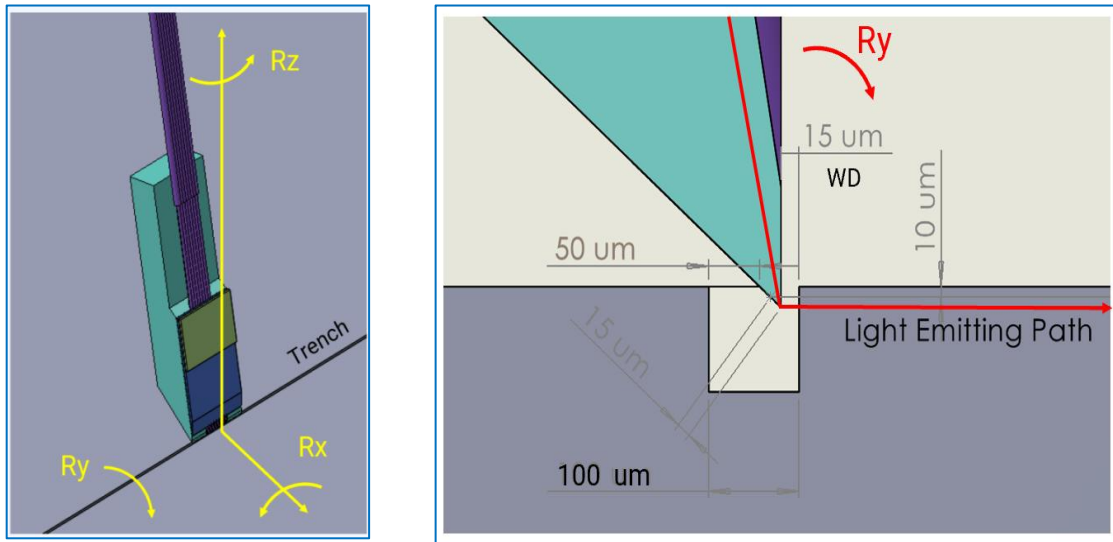


Figure 1: Polished FAU as the optical probe for wafer-level PIC tests. The FAU angles need to be optimized to ensure safe insertion into the trench, correct direction for the light path, and precise alignment of the fiber channels to the optical ports on the wafer.

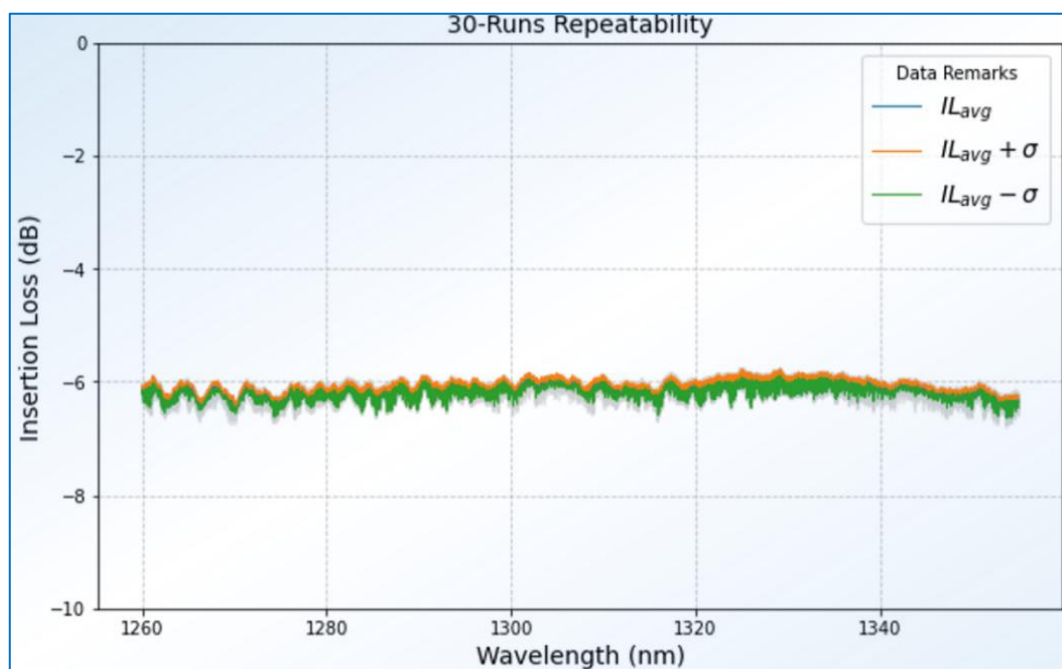


Figure 2: A loopback reference structure with edge couplers is measured 30 times for insertion loss. The results show high repeatability with a standard deviation $\sigma < 0.1$ dB which is required for automated wafer test.

Although the FAU is usually composed of single-mode fibers with a mode field diameter (MFD) around $10\text{ }\mu\text{m}$, which may not perfectly match the MFD of the on-wafer edge coupler, this mismatch leads to a predictable and repeatable coupling loss. Such loss can be measured, calibrated, and subtracted as a consistent reference in subsequent tests. Figure 2 demonstrates the high repeatability of insertion loss measurements for a "loopback" reference structure with edge couplers. The measured total insertion loss is 6 dB, which corresponds to a coupling loss of 3 dB per facet. This reference measurement serves as a baseline: in subsequent tests of other PIC devices, the coupling loss can be systematically subtracted, allowing the true insertion loss of the device under test to be accurately determined.

Another remarkable feature of the polished FAU is in its excellent stability, as demonstrated by its optical power fluctuation remaining within 0.1 dB over a 30-minute period (Fig. 3). This level of performance ensures consistent coupling and measurement reliability, even during extended automated test sequences.

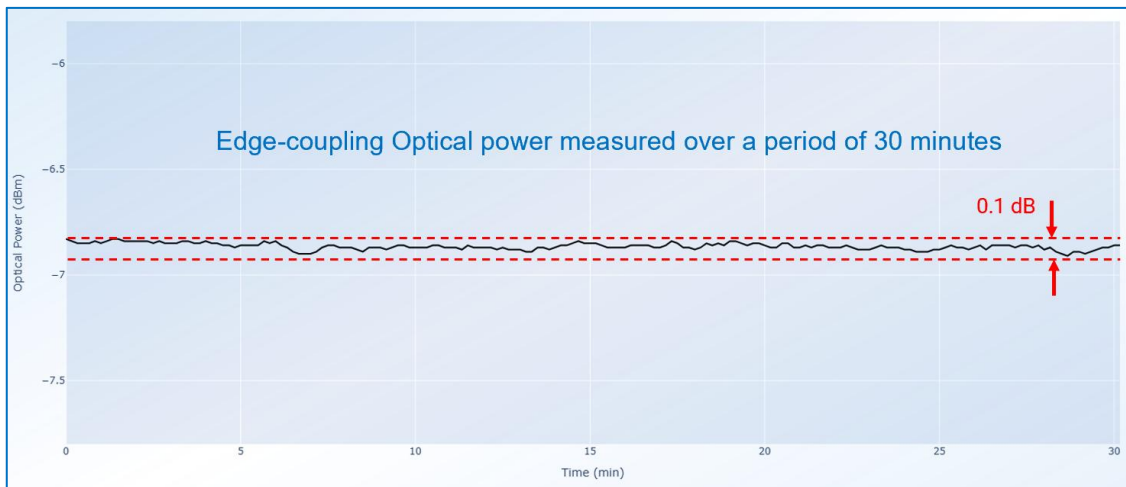


Figure 3: The optical power measured with polished FAU show fluctuations less than 0.1 dB over a time frame of 30 minutes.

3. Motion Stage

Test systems for PIC wafers must account for a range of compound errors that significantly impact alignment consistency and test reliability—issues that are often negligible or more manageable in single-die testing environments. At the wafer level, where dozens or hundreds of dies must be characterized in succession, even small deviations in alignment or setup can result in large measurement variability and misinterpretation of device performance.

Standard wafer probes are typically optimized for electrical contact testing and may lack the angular resolution, mechanical stability, or repeatability necessary for precise optical alignment. At wafer scale, the cumulative effect of minor positioning errors leads to inconsistent fiber-to-device alignment, which can skew comparisons across dies.

Accurate localization of optical features—such as dicing trenches, waveguide facets, or alignment marks—often relies on top-view cameras. However, variations in illumination, focus, contrast, and surface reflectivity degrade the accuracy of visual detection. These inconsistencies are amplified during automated alignment routines, especially when transitioning from one reticle to another across the wafer.

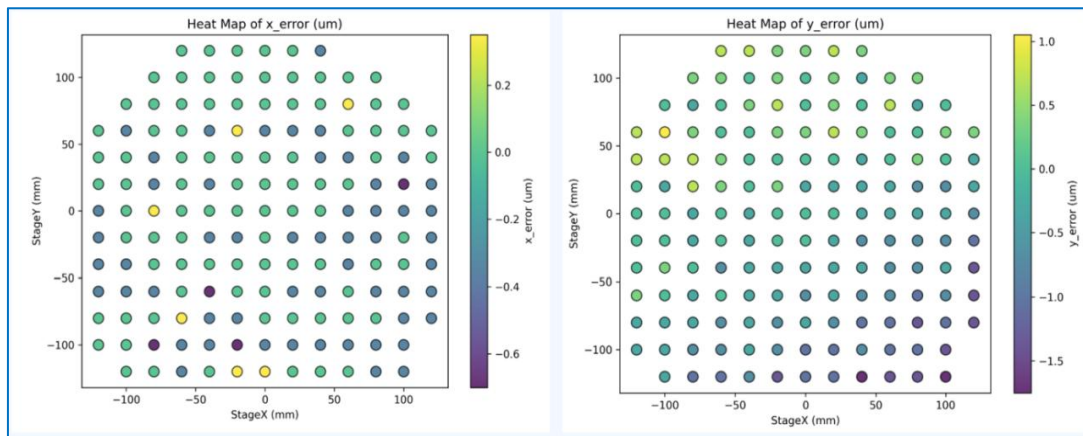


Figure 4: A typical mapping of positioning errors in the x-direction (left panel) and y-direction (right panel) across the probe station stage. High positioning accuracy of 1–2 μm is required to maintain a consistent coupling distance across the wafer, ensuring data reliability and preventing collisions with the trench walls.

Unlike in isolated die testing where the optical probe height can be finely adjusted per device, wafer-level testing demands a system that maintains consistent fiber-to-device distance across the entire wafer. This coupling distance directly affects insertion loss and test repeatability. Factors such as wafer warpage, local topography, and chuck flatness further complicate Z-axis control, making it difficult to ensure that each device is tested under identical coupling conditions. The transition from single-die to wafer-level testing introduces a need for far tighter control over stage motion, vision-based localization, and vertical alignment—without which meaningful wafer-scale comparisons become unreliable. High positioning accuracy of 1-2 μm is therefore required for wafer-level PIC tests (Fig. 4).

4. Wafer-Level Variations

Even with optimal mechanical and optical alignment, test engineers frequently observe measurement inconsistencies that stem from wafer-level variations. These are often difficult to diagnose and even harder to control. The dominant variations in silicon photonics are silicon thickness and feature size [Refs. 2, 8]. These variations

appear from wafer to wafer, as well as within a single photonic integrated circuit. Across the wafer, small lithographic errors, or planarization non-uniformities can result in positional offsets of photonic structures from one reticle to another (Fig. 5). These shifts alter the expected fiber-to-port alignment, requiring constant re-alignment and increasing the risk of coupling inconsistencies—particularly in automated testing environments where manual correction is impractical.

Inaccurate or inconsistent compensation for these shifts introduces variable coupling losses across the wafer, making it difficult to distinguish whether a measured loss is due to the photonic device itself or to a misalignment or coupling artifact. To isolate the true optical characteristics of PIC devices, it becomes essential to reliably and repeatedly measure the coupling efficiency at each site, and to decouple it from the device's intrinsic performance. This often requires incorporating reference structures, advanced calibration routines, or machine learning techniques to separate optical probe-induced loss from actual device response.

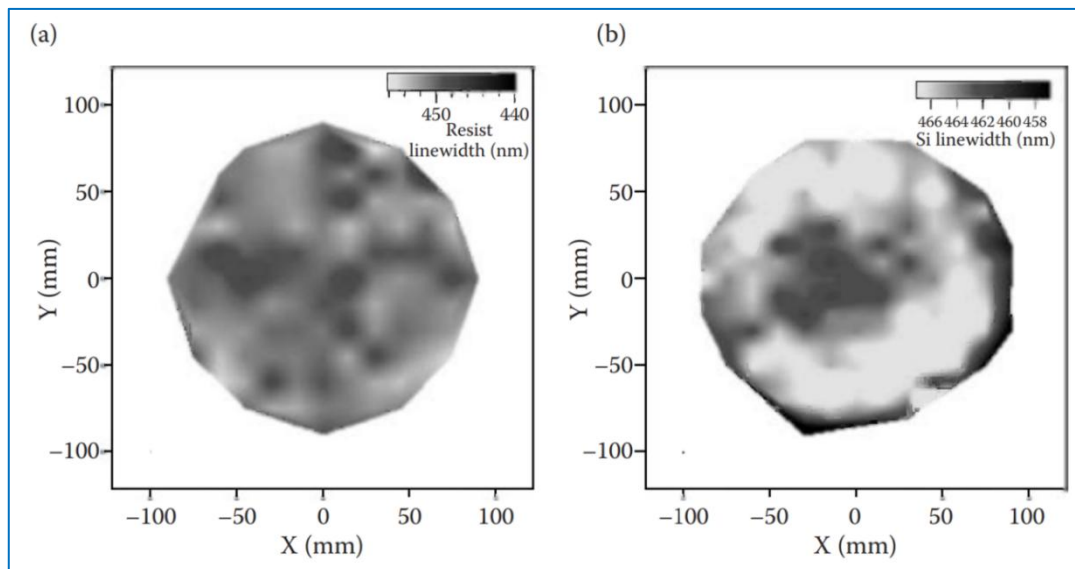


Figure 5: Photoresist linewidth uniformity after projection photolithography (a) and silicon waveguide linewidth after etch (b). Taken from [Ref. 2]

Moreover, wafer-scale process parameter variations—such as non-uniform etching, layer thickness drift, or doping fluctuations—can legitimately cause variations in optical device performance across the wafer. However, unless coupling loss is properly accounted for and removed, these intrinsic variations may be masked or misinterpreted as alignment errors. Without careful decoupling of optical path loss and device-specific performance, engineers risk drawing incorrect conclusions about design quality, process stability, and yield. Ensuring that detected variability reflects actual device characteristics, rather than systematic test inconsistencies, is therefore fundamental to reliable PIC production and PDK validation.

5. System Complexity

Introducing optical testing into established wafer-level test environments presents significant system-level challenges that go beyond simply adding new hardware. Coordinating measurements across optical, electrical, thermal, and mechanical domains requires precise timing, hardware triggering, and software orchestration. This often demands custom integration layers to unify disparate systems, which can significantly increase development overhead.

Optical testing workflows rely on a tightly interwoven software stack encompassing calibration routines, vision-based alignment, real-time signal acquisition, and motion control. Ensuring stable communication between these subsystems—especially in high-throughput scenarios—requires robust architecture, rigorous error handling, and careful version control.

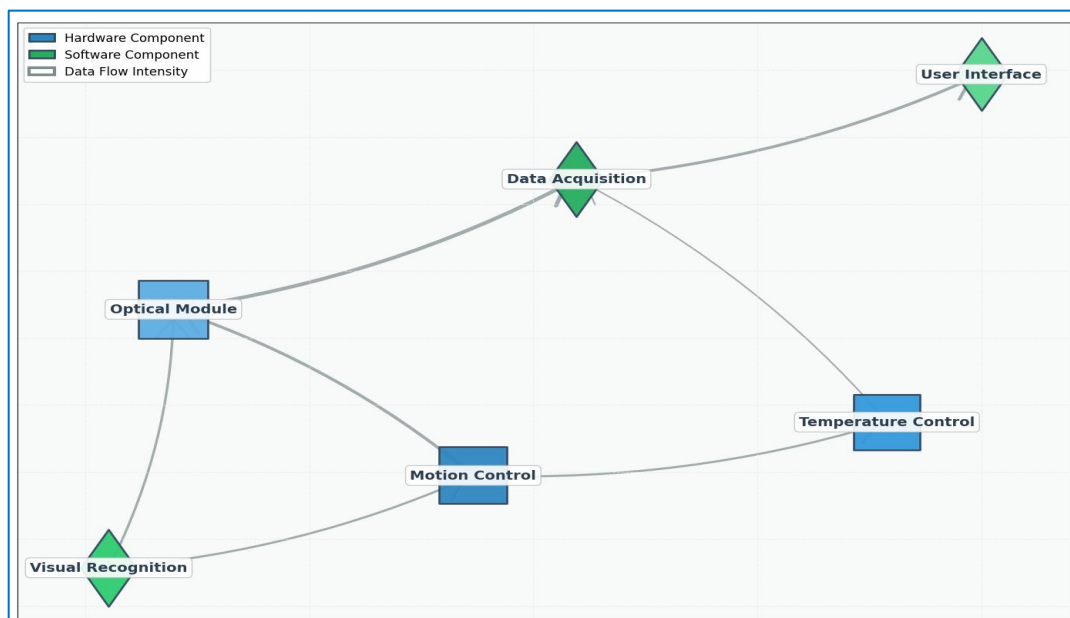


Figure 6: A simplified illustration of multi-domain test system interaction network in wafer-level PIC testing.

Navigating these complexities demands more than just hardware — it requires an intelligent, robust software backbone. *Navigo*, Sunyu's proprietary PIC test integration software, was purpose-built to unify the multi-domain challenges of optical wafer testing (Figures 7A & 7B). *Navigo* seamlessly manages complex interactions between motion stages, optical probes, electrical instruments, and vision systems, ensuring coordinated operation across optical, electrical, mechanical, and thermal domains. Core functions include real-time motion orchestration, vision-guided fiber alignment, automated pivot-point calibration, dynamic wafer mapping, and flexible equipment triggering, all integrated under a unified software framework designed for high throughput and robust error resilience.

At the heart of Navigo is a highly modular, scalable architecture that directly controls probe station, optical and electrical probes, vision inspection modules, and test equipment such as tunable lasers, optical power meters, sourcemeter, vector network analyzer, bit error ratio tester (BERT), and so on. It is worth noting test instruments of any brand can be integrated into Navigo due to its open architecture. Sunyu has been in partnership with major brands of test instruments to include their test instruments in wafer-level PIC tests.

For optical probing, Navigo incorporates proprietary algorithms that dynamically determine and update the fiber pivot point, along with high-speed active alignment algorithms to meet high-throughput requirements.

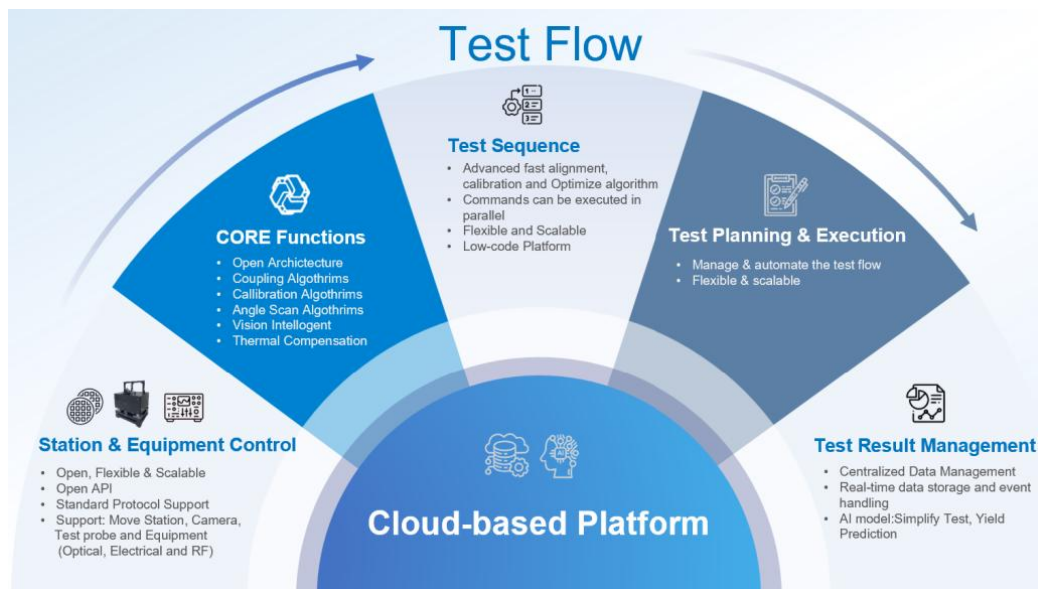


Figure 7A: Illustration of Navigo's modular and scalable architecture dedicated to enable complex PIC wafer level testing.

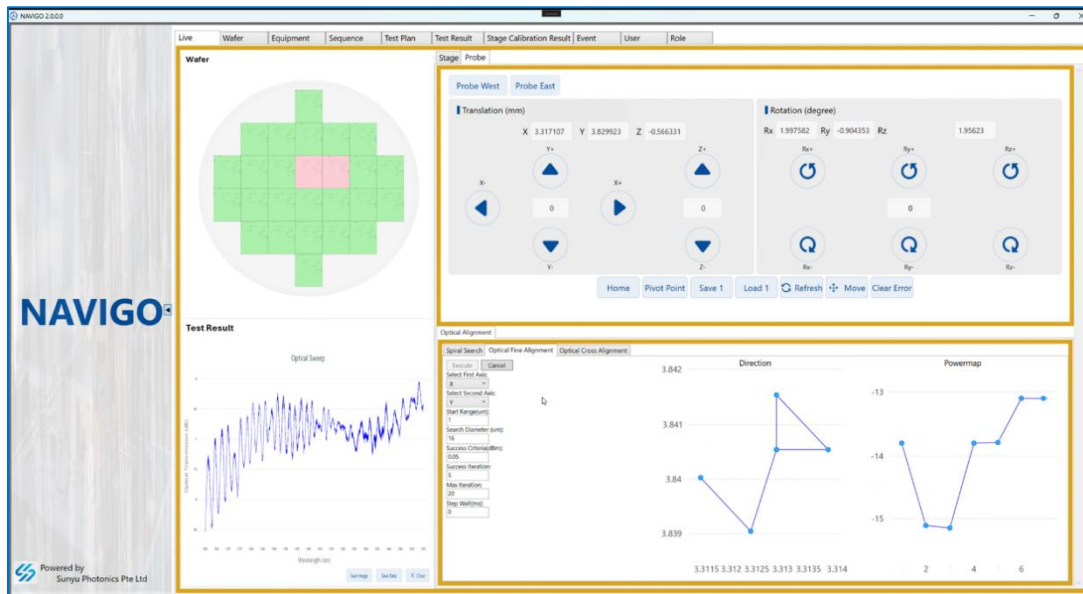


Figure 7B: Navigo User Interface for Wafer-Level Photonic Testing

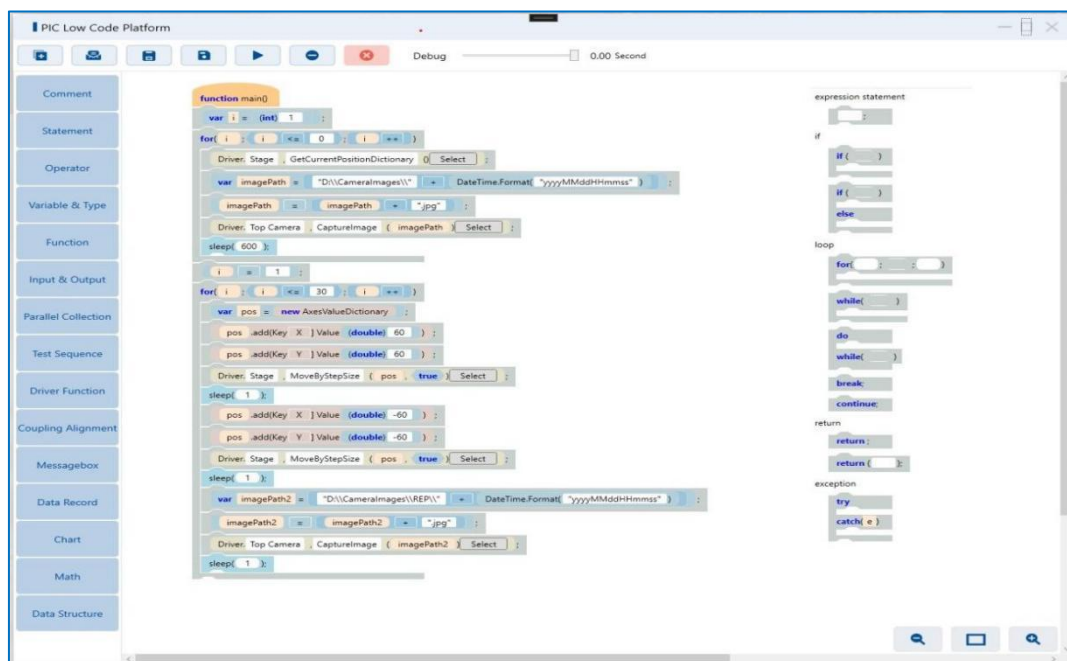


Figure 8: Navigo's low-code platform enables engineers to easily build and edit sequence for automated PIC wafer tests.

Navigo further distinguishes itself with its low-code test sequence engine, allowing engineers to construct complex test flows — including wavelength sweeps, polarization optimization, optical-electrical parameter extraction, and batch wafer testing — through a graphical interface without writing extensive code. Sequences can trigger synchronized movements, measurements, and data logging, tightly controlling timing across all subsystems. Native support for industrial communication

standards (such as TCP/IP, GPIB, RS-232) and an open API framework ensure that Navigo can integrate seamlessly with third-party instruments, enabling flexible system expansion as new testing needs arise.

To enhance operational robustness, Navigo embeds advanced error handling, logging, and recovery mechanisms at every layer. This includes real-time stage position monitoring and auto-connect strategies for communication failures. Combined with comprehensive data management and visualization tools, Navigo not only automates the complexity of wafer-level optical probing but also provides deep insights into system performance and device behaviour. By abstracting hardware intricacies into a unified, user-friendly platform, Navigo empowers test engineers to achieve rapid deployment, high repeatability, and scalable production testing in the demanding environment of PIC manufacturing.

6. Calibration Process

Figure 9 shows that the automated wafer-level edge coupling system requires a multi-step calibration process to ensure high-precision alignment between the fiber array unit (FAU) and the photonic integrated circuit (PIC) under test. Top-camera calibration is first performed to determine the global coordinate system and angular orientation of the imaging system, enabling accurate machine vision alignment. Next, stage calibration ensures that the stage positioning achieve high positioning accuracy $< \pm 1.5 \mu\text{m}$ (Figure 10), not only to prevent collisions between the FAU and wafer, but to maintain consistent working distance across all devices under test (DUTs). The stage calibration can be performed using a standard calibration wafer with accurate placement of patterns across the wafer as well as using the actual PIC wafer to be tested. Wafer calibration identifies the global center and rotation angle of the wafer under test, allowing for the precise mapping of DUT coordinates for automated probing. Following this, Z-planarity calibration is executed after each new wafer is loaded. Specifically, Sunyu's proprietary algorithm samples 200–250 points across the wafer surface to determine the local Z-height and compensates for Z-height variations during testing (Figure 11). This Z-planarity calibration remains valid for wafers of the same batch as long as they share the same warpage characteristics.

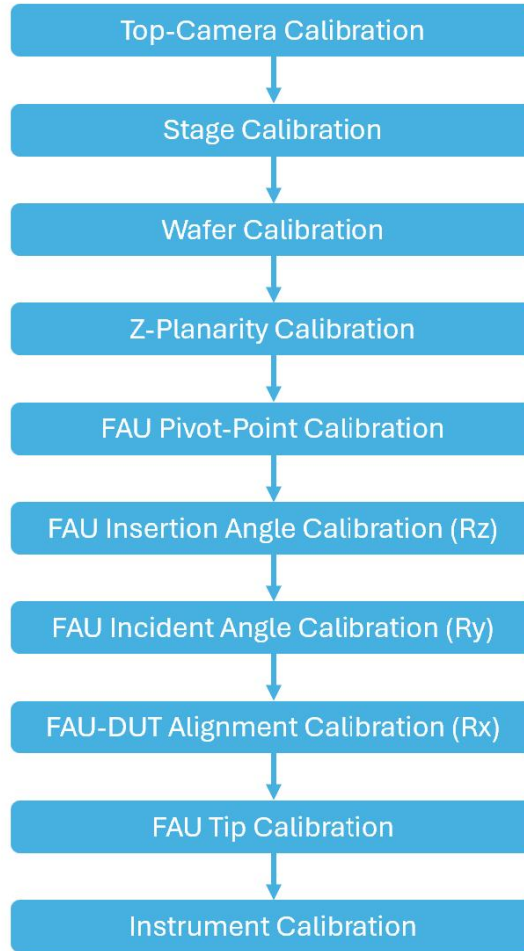


Figure 9: A series of calibration process is performed by Sunyu system to enable PIC wafer level test.

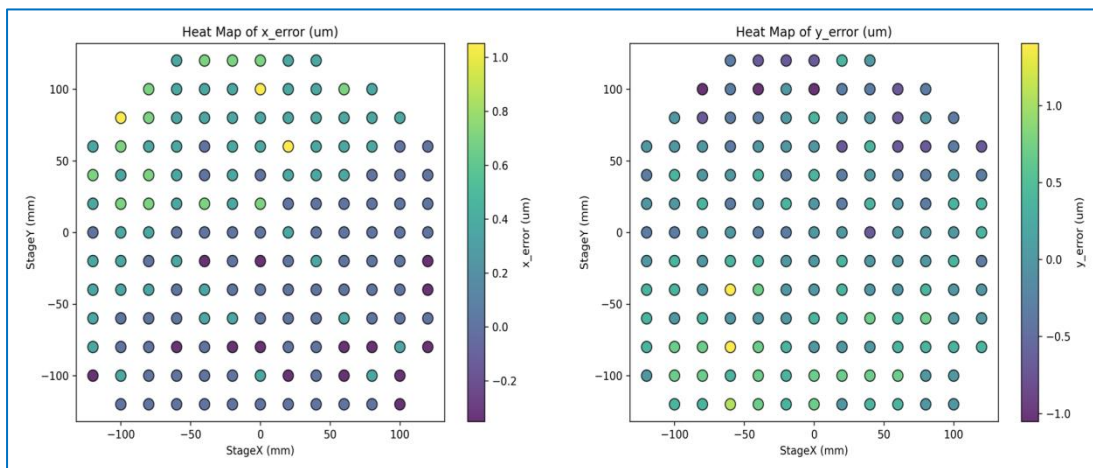


Figure 10: Heat maps representing high positioning accuracy $< \pm 1.5 \mu\text{m}$ for the X-axis (left panel) and Y-axis (right pane;) following the stage calibration function of the Sunyu system. This level of precision ensures consistent and repeatable fiber-to-chip alignment across the wafer.

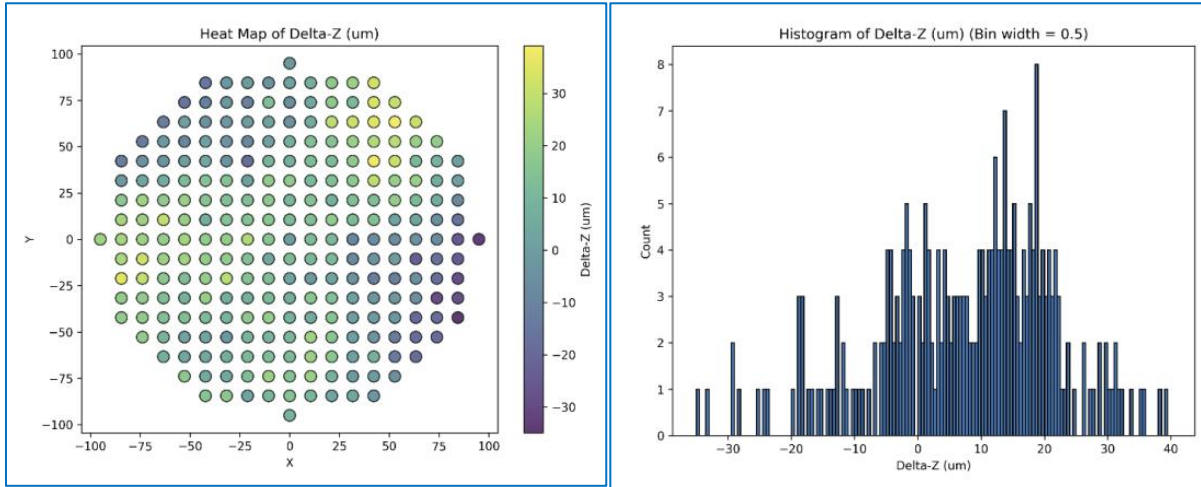


Figure 11: Local Z-variations relative to the wafer center were measured uniformly across the wafer surface following the Z-planarity calibration function of the Sunyu system. The resulting heat map (left panel) and histogram (right panel) reflects the effective wafer warpage after placement on the chuck. These height deviations will be compensated by the system during wafer-level automated testing, ensuring consistently fast and accurate alignment despite non-uniform wafer surface topology.

A critical step, FAU pivot-point calibration, addresses the inherent collision risk during optical probe insertion. Every motion of the optical probe carries a chance of fiber damage or wafer surface abrasion if angular adjustments are not pivoted correctly. The pivot-point calibration is to determine a virtual pivot point—the spatial origin about which rotations (Rx, Ry, Rz) can be made without translating the fiber tip.

At Sunyu, the engineer is assisted by proprietary software algorithm to determine the pivot point using a high precision 6-axis manipulator that controls the optical probe's position and orientation across six degrees of freedom (x, y, z, Rx, Ry, Rz). Small-angle rotations around the selected local axis (Rx, Ry, or Rz) are performed by adjusting the manipulator, mathematically represented by a two-dimensional rotation matrix:

$$R = \begin{pmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{pmatrix}$$

where θ is the rotation angle. After each rotation, the fiber tip undergoes compensatory translations, and the updated pivot point is recalculated and the difference from the previous estimate is evaluated using:

$$\Delta P = \sqrt{(x_{new} - x_{old})^2 + (y_{new} - y_{old})^2 + (z_{new} - z_{old})^2}$$

Convergence is achieved when ΔP falls below a preset threshold, typically on the order of one micron, and the pivot point is fully determined. This ensures that subsequent angular adjustments can be made without lateral drift of the fiber tip, greatly reducing the risk of wafer contact and maintaining high-precision optical coupling.

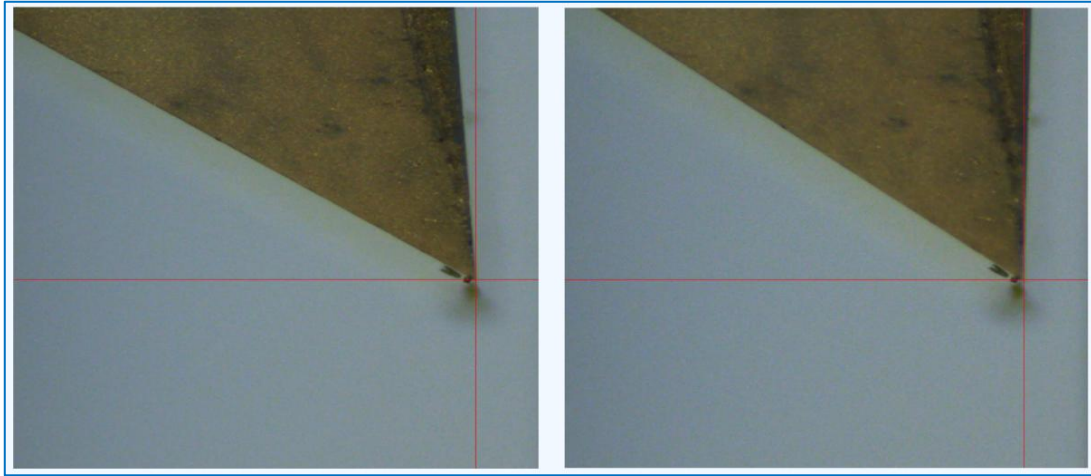


Figure 12: Pivot-point function is required to enable the rotation of FAU safely above a wafer while mainlining the distance between the two objects.

With the pivot point activated, subsequent angular calibrations for the FAU include (a) insertion angle (R_z), which ensures the FAU is parallel to the coupling trench, minimizing contact risk and maintaining consistent insertion depth, (b) Incident angle (R_y) calibration adjusts the probe to ensure the input light propagates horizontally into the waveguide, and (c) FAU-DUT alignment (R_x) calibration aligns the entire fiber array with the edge couplers to reduce the need for individual fiber alignment. Finally, FAU tip calibration determines the Z-position of the fiber tip, ensuring safe automated operation without fiber-wafer collision. Through this structured calibration sequence, Sunyu establishes a robust, repeatable foundation for high-throughput wafer-level PIC testing.

Equally important is the instrument calibration. Depending on the measurement configuration, different calibration approach is needed. Figure 13 shows a typically configuration for the measurement of four-channel coarse wavelength division multiplexer devices (CWDM). Four optical paths are present in the setup. Each of their system loss needs to be referenced out to measure the actual insertion loss of the DUTs.

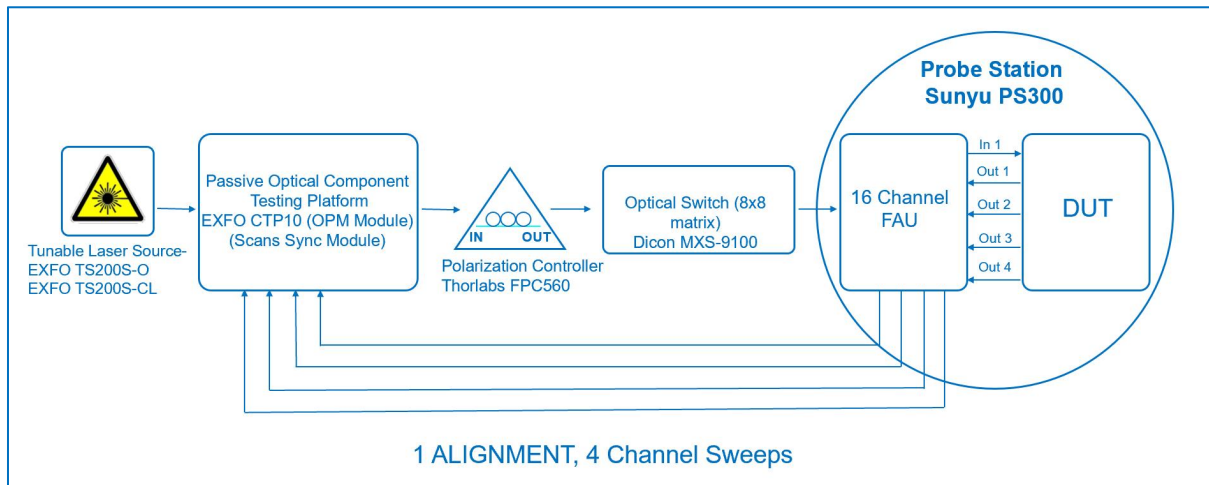


Figure 13: A typical measurement setup for insertion loss characterization of a four-channel coarse wavelength division multiplexer (CWDM).

The abovementioned calibration process, powered by Sunyu’s proprietary algorithms, ensures that wafer-level tests are consistently performed under a well-calibrated state. This allows the system to deliver highly repeatable and reliable results—even when the wafer is reloaded at a later time. Figure 14 illustrates this robustness, showing consistent measurements from nine test runs conducted across three separate wafer loadings. This capability reflects the state-of-the-art performance in automated PIC edge-coupling testing.

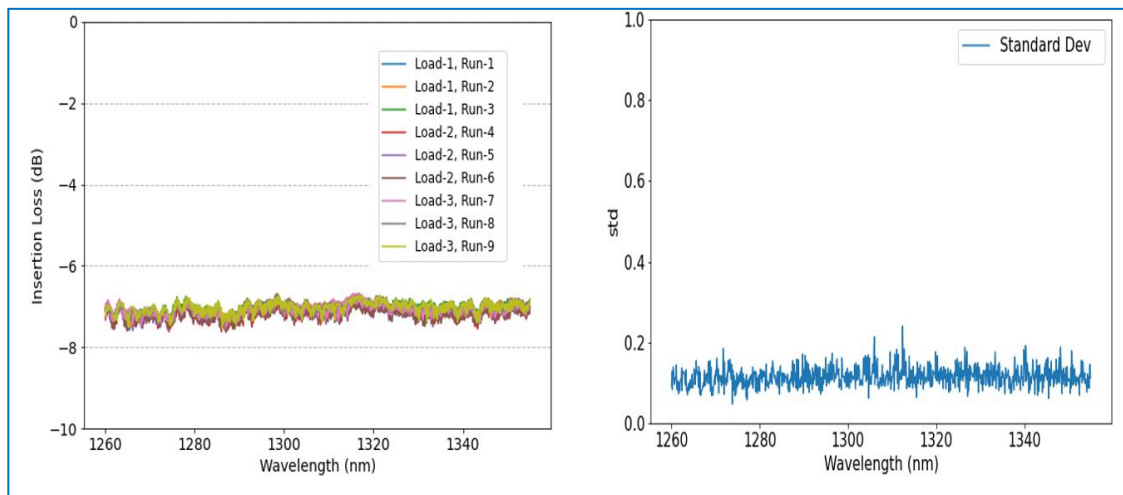


Figure 14: Insertion loss measured at one test point over 9 runs, across three different wafer loadings (left), shows very consistent results. The right graph shows the standard deviation over the 9 runs, which stays below 0.2 dB across the wavelength range. This demonstrates that the Sunyu system provides stable and repeatable results, even when the wafer is reloaded.

7. Test Throughput

Wafer-level testing of photonic integrated circuits (PICs) confronts a core dilemma: how to maximize test throughput while maintaining the accuracy and reliability of measurements. This balance is particularly challenging in optical testing, where physical coupling intricacies and environmental sensitivities significantly impact performance metrics.

Optical coupling efficiency is highly sensitive not just to lateral and vertical positioning (Fig. 15), but also to angular orientation—often down to the millidegree level. Unlike electrical probes that operate largely perpendicular to the wafer, optical probes must approach at specific, non-orthogonal angles that match the orientation of waveguide facets or grating couplers. Adjusting these angles without colliding with the wafer surface or damaging the fiber tips demands precise mechanical control and real-time feedback, neither of which are standard in most test setups.

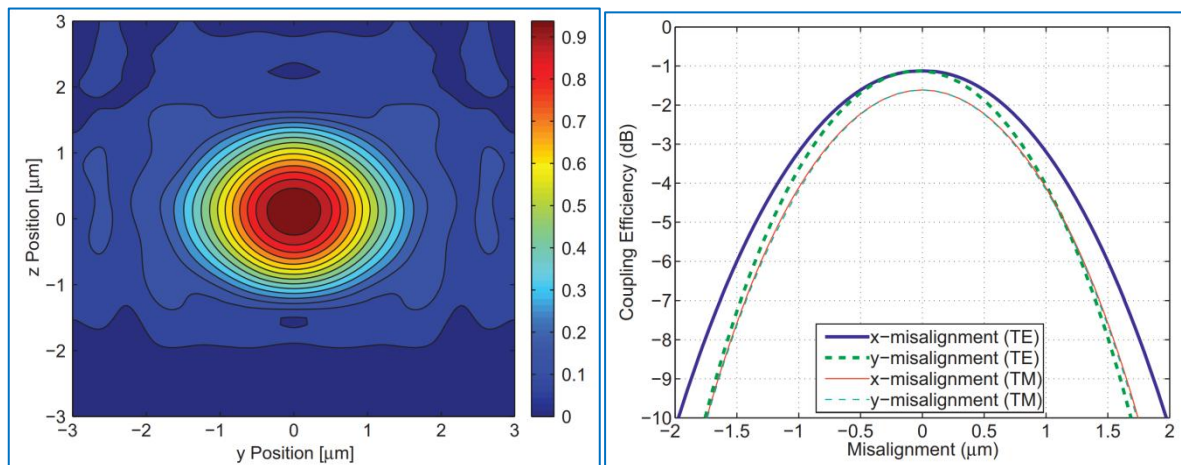


Figure 15. Left panel: FDTD simulation of the nano-taper edge coupler – field profile at the output, in air: x-axis tangential waveguide; y-axis, surface normal to wafer. Nano-taper length 200 μm , with 180×220 nm tip, $\lambda = 1.55$ μm , quasi-TE polarization. Right panel: Mode overlap calculations showing power coupling efficiency versus misalignment (x, y): 180×220 nm nano-taper, $\lambda = 1.55$ μm , quasi-TE polarization. Figures taken from [Ref 1].

Optimal optical alignment is required for each device. This fine-tuning can be time-consuming and difficult to automate reliably, especially when each die may present subtle variations in surface topology or grating coupler orientation. As a result, the alignment process becomes a bottleneck in the overall test cycle, hindering throughput and limiting test coverage (Fig. 16).

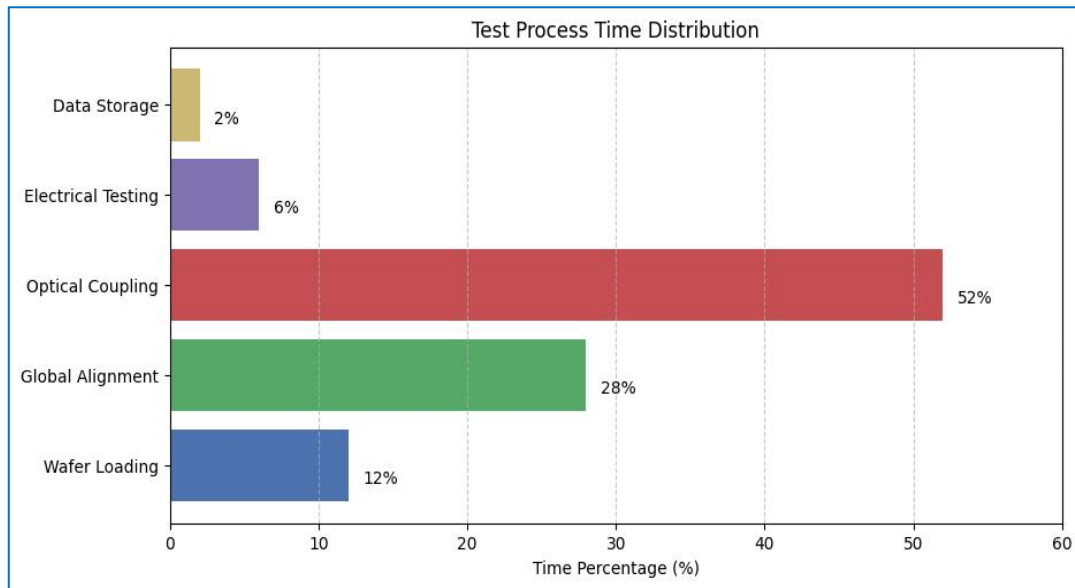


Figure 16: Typical test process time distribution in PIC wafer testing.

At Sunyu, a proprietary gradient-search algorithm is employed to achieve high-speed coupling alignment, typically completing the process within 3 to 4 seconds. The alignment can be conceptualized as a localized search for the optical power maximum, where the fiber array unit (FAU) probes the surrounding region to identify the point of highest coupling efficiency (Fig. 17). The algorithm intelligently guides the FAU through iterative adjustments, continuously improving optical power at each step and accurately determining when the optimal alignment has been reached (Fig. 18). It is designed to be both fast and robust, capable of recovering optical coupling even in scenarios where the initial alignment suffers from losses of several tens of dB. This reliable and efficient alignment process significantly enhances overall test throughput—an essential factor for scalable, production-grade wafer-level photonic testing.

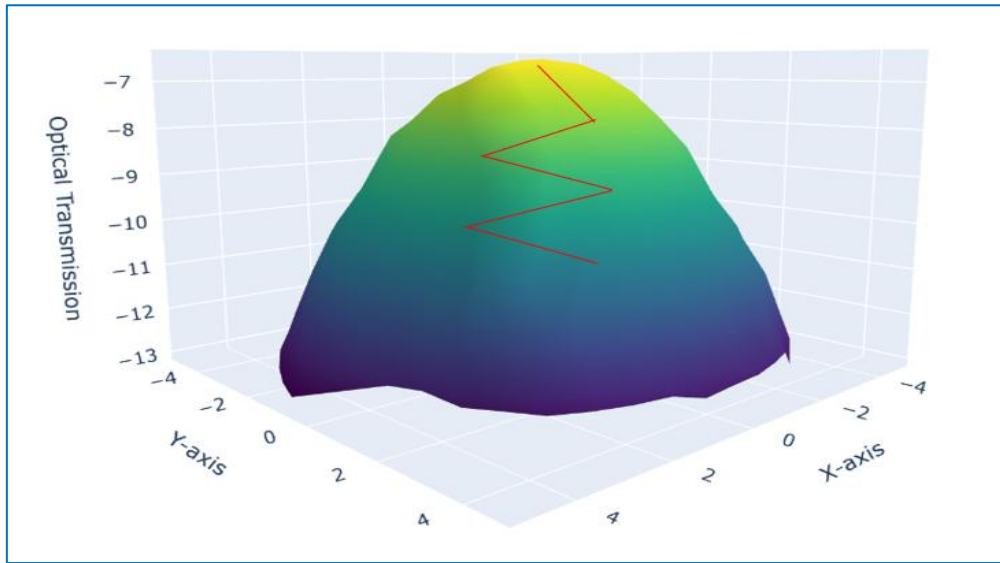


Figure 17: The optical alignment is a high-precision process on the sub-micron level.

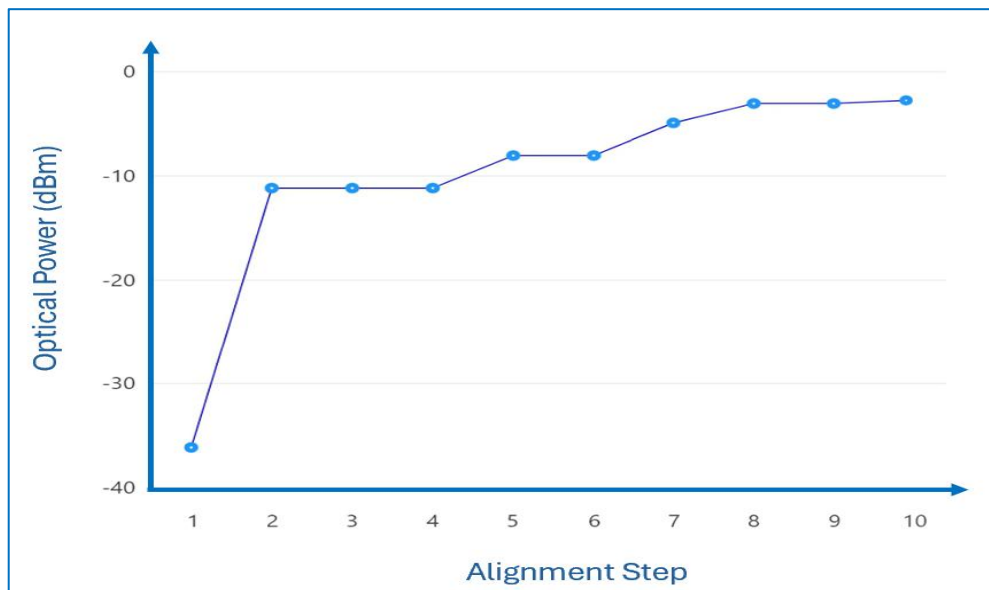


Figure 18: The FAU optical power gets optimized with Sunyu proprietary coupling alignment algorithm.

To demonstrate the fast alignment for high-throughput performance, wafer-level edge-coupling tests were performed on 52 dies evenly distributed across an 8-inch photonic integrated circuit (PIC) wafer. Using the Sunyu PS-300 system, the tests were repeated over 10 runs, amounting to automated testing of 520 dies per wafer. Insertion loss was measured at each point. The total test duration was 2 hours and 5 minutes, translating to approximately 14 seconds per test site—including stage movement, FAU alignment, and measurement. Figure 19 shows one of the test results. This demonstrates how the fast and repeatable alignment algorithm directly contributes to practical wafer-scale testing throughput, making it viable for both high-volume production and iterative R&D workflows.

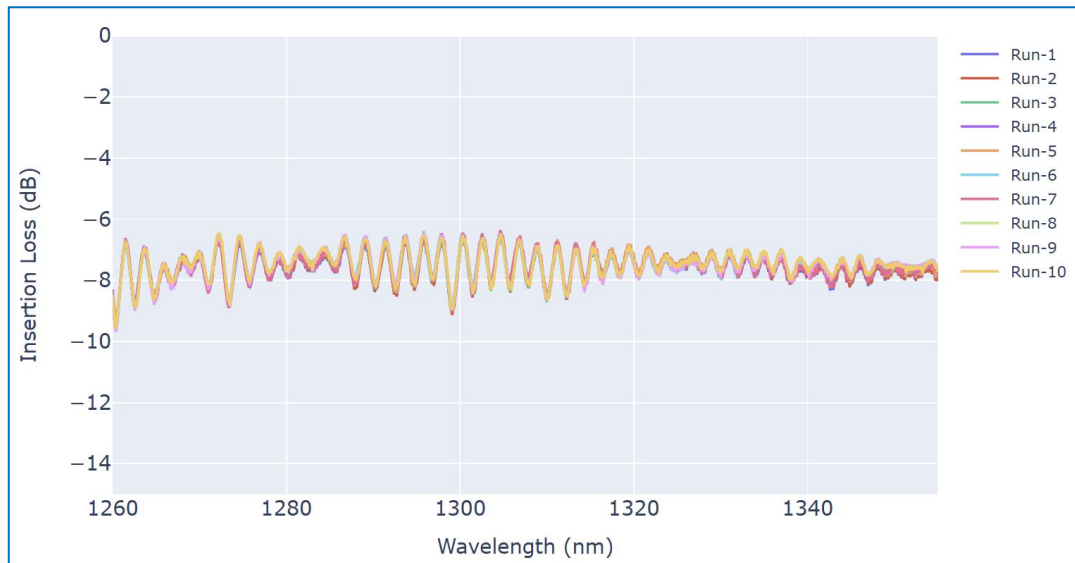


Figure 19: Insertion loss measured at one of the 52 test points across 10 consecutive wafer-level runs spanning 2 hours and 5 minutes. The consistency of the results further confirms the reliability and repeatability of the Sunyu system.

Unlike electrical testing—where well-established standards, robust probe cards, and streamlined automation flows support efficient production—optical testing lacks universally adopted protocols. The absence of standardization across equipment vendors and test methodologies limits the scalability of optical probing systems. This is particularly problematic in research and development environments or in pilot production, where diverse device types and rapidly evolving designs require flexible yet consistent testing strategies.

Ultimately, overcoming this throughput-accuracy trade-off will require innovations in optical probe design, smarter alignment algorithms, better real-time feedback mechanisms, and tighter integration of test software and hardware. Without such advancements, wafer-level PIC testing will remain a rate-limiting step in the broader photonics manufacturing pipeline.

Conclusion

Wafer-level testing for PICs introduces a host of challenges that go beyond electrical probing. From FAU alignment intricacies to test repeatability and calibration dependencies, the field demands not only new tools but a new mindset. Test engineers venturing into this domain must prepare for a multi-disciplinary approach combining optics, precision mechanics, machine vision, and system-level software control.

The Sunyu PS300 represents a new standard for fully automated wafer-level photonic integrated circuit (PIC) testing. Designed specifically for the unique

demands of edge-coupling and grating-coupling tests, the PS300 delivers sub-micron positioning precision, high mechanical stability, and fast alignment speeds across full 8" and 12" wafers. Its modular platform combines six-axis optical probe control, vision-based alignment, flexible electrical probing, and integrated control, all orchestrated by Sunyu's proprietary Navigo software. Built for both R&D and production environments, the PS300 minimizes human intervention, enables high-throughput automated test flows, and provides the reliability and repeatability required for rigorous process validation, PDK development, and volume manufacturing. With proven performance in wafer-scale optical coupling, the PS300 empowers users to accelerate time-to-data, improve yield analysis, and streamline the entire photonic device characterization workflow.

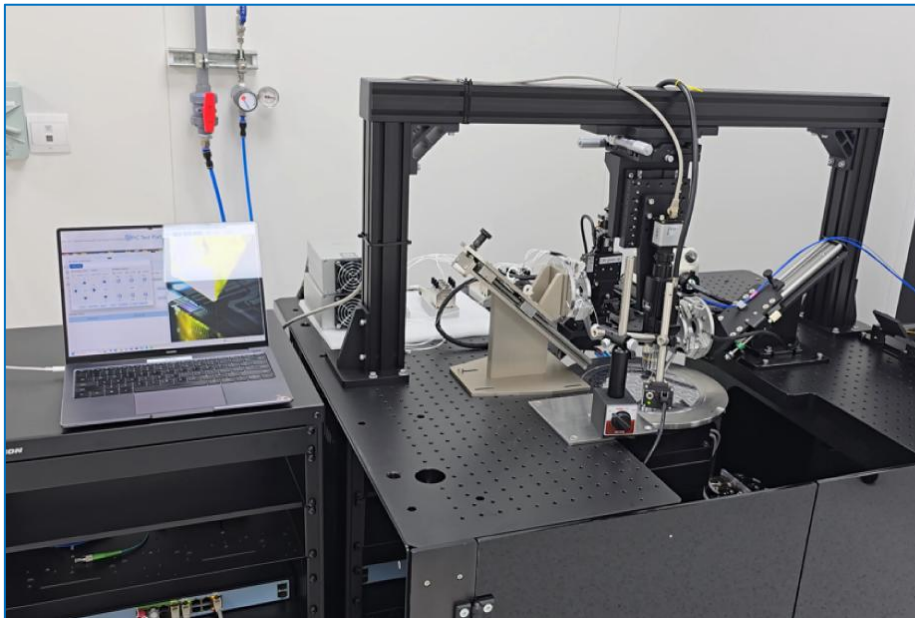


Figure 20: Sunyu offers fully automated probe system for photonic wafer testing to support your R&D as well as lab-to-fab production scale-up.

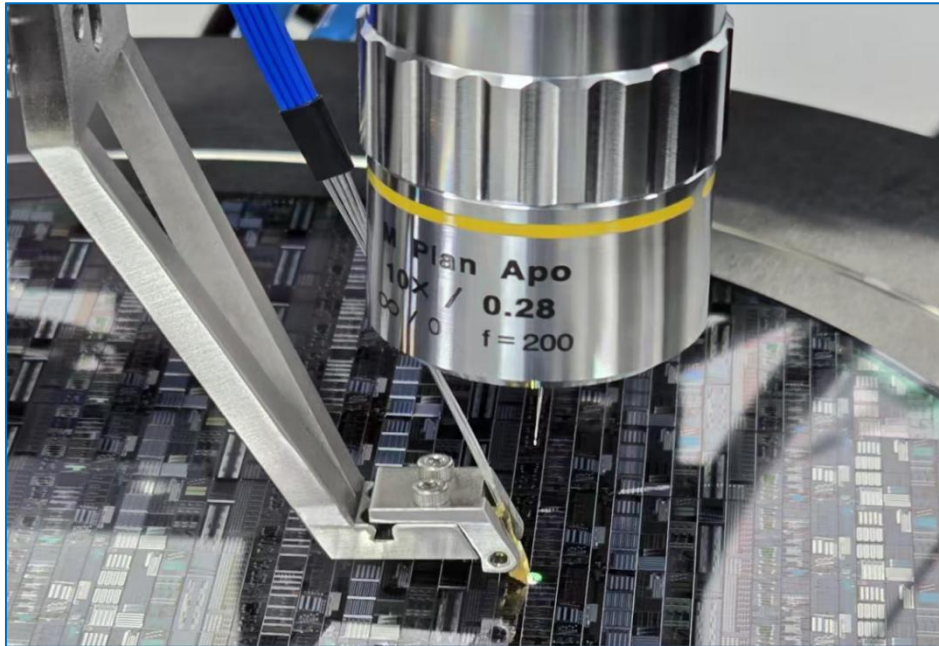


Figure 21: Close up view of the FAU mounted on probe arm.

To further enhance automation and minimize human involvement in repetitive, high-risk handling tasks, Sunyu recommends integrating the fully automated Wafer Loader Unit into production-level setups. Manual wafer exchange not only introduces variability and handling-induced risks such as wafer misalignment, contamination, or warpage, but also becomes a major source of cycle time inefficiency. The wafer loader supports industry-standard 8" SMIF, 12" FOUP, and open cassette formats, enabling seamless cassette-to-chuck transfer, wafer mapping, double wafer detection, and warpage inspection — all without operator intervention. In high-throughput environments where consistency, repeatability, and safety are paramount, automation of the wafer loading process helps eliminate operator error, streamline test cycles, and enforce traceability standards, making it an indispensable component of scalable, production-grade PIC wafer test systems.

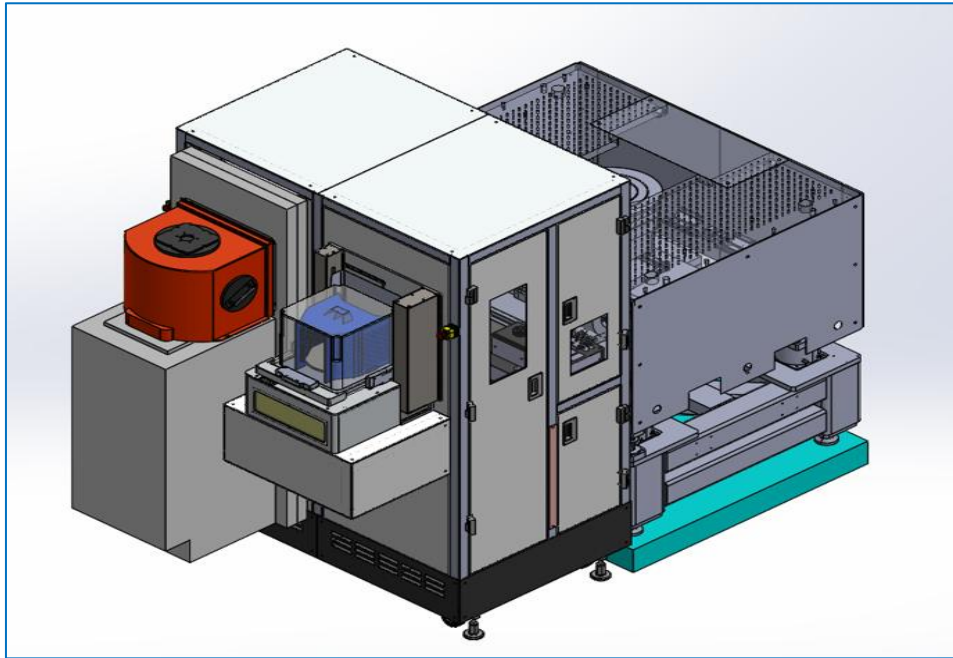


Figure 22: The Wafer Loader Unit is an upgrade option for the PS300, supporting industry-standard 8" SMIF pods, 12" FOUPs, and open cassette formats.

At **Sunyu Photonics**, we're here to help you navigate this complexity. With deep expertise in photonics testing, automation, and system integration, we provide the tools, solutions, and support needed to overcome these challenges—whether you're in R&D, pilot production, or scaling to high-volume manufacturing. Let us partner with you to accelerate your PIC development and ensure test reliability at every stage.

References

1. Silicon Photonics Design: From Devices to Systems [2015], L. Chrostowski and M. Hochberg
2. Handbook of Silicon Photonics [2013], Edited by L Vivien and L. Pavesi
3. Wafer-scale high-density edge coupling for high throughput testing of silicon photonics [2018], R. Polster et al.
4. Edge-Coupled Active and Passive Wafer-Scale Measurements on 300mm Silicon Photonics Wafers [2021], K. M. Jabon et al.
5. Robust Edge Coupling Probe Applied in Wafer-Level Optical Testing [2023], S.-H. Huang et al.
6. 3D-Printed Optics for Wafer-Scale Probing [2018], M Trappen et al.
7. 3D-printed optical probes for wafer-level testing of photonic integrated circuits [2020], M Trappen et al.
8. Review of Silicon Photonics Technology and Platform Development [2021], S. Y. Siew et al.

Sunyu Patents

To advance photonic integrated circuit (PIC) wafer testing and better support the growing needs of the industry, Sunyu has developed a series of patented test technologies. These innovations are developed to enhance alignment precision, improve repeatability, and enable high-throughput, wafer-level testing—key enablers for both R&D and volume production in the photonics sector.

Application No: 10202500586R

METHOD AND APPARATUS FOR DETERMINING ROTATION CENTER POINT
IN OPTICAL FIBER MOVING PROCESS, DEVICE AND MEDIUM

Application No: 10202500585V

WAFER POSITION CALIBRATION METHOD AND APPARATUS, READABLE
STORAGE MEDIUM AND DEVICE

Application No: 10202500584S

EXPANSION OFFSET CALIBRATION METHOD AND APPARATUS,
READABLE STORAGE MEDIUM AND DEVICE

Application No: 10202501544Y

METHOD, SYSTEM, DEVICE, AND MEDIUM FOR FAU ANGLE CALIBRATION IN
PHOTONIC INTEGRATED CIRCUIT TESTING

Application No: 10202501545X

METHOD, SYSTEM, MEDIUM, AND DEVICE FOR INSERTING FIBER ARRAY
UNIT INTO THE EDGE-COUPPLING TRENCH OF A PHOTONIC INTEGRATED
CIRCUIT(PIC) WAFER